Data Sheet | November 1999 | File Number 480.5

General Purpose High Current NPN Transistor Arrays

CA3081 and CA3082 consist of seven high current (to 100mA) silicon NPN transistors on a common monolithic substrate. The CA3081 is connected in a common emitter configuration and the CA3082 is connected in a common collector configuration.

The CA3081 and CA3082 are capable of directly driving seven segment displays, and light emitting diode (LED) displays. These types are also well suited for a variety of other drive applications, including relay control and thyristor firing.

Ordering Information

PART NUMBER (BRAND)	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
CA3081	-55 to 125	16 Ld PDIP	E16.3
CA3081F	-55 to 125	16 Ld CERDIP	F16.3
CA3081M (3081)	-55 to 125	16 Ld SOIC	M16.15
CA3082	-55 to 125	16 Ld PDIP	E16.3
CA3082M (3082)	-55 to 125	16 Ld SOIC	M16.15
CA3082M96 (3082)	-55 to 125	16 Ld SOIC Tape and Reel	M16.15

Features

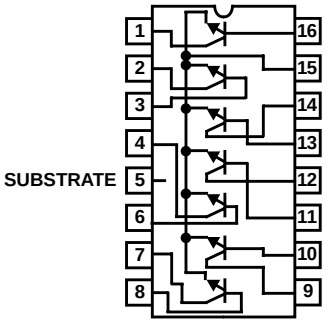
- CA3081 - Common Emitter Array
- CA3082 - Common Collector Array
- Directly Drive Seven Segment Incandescent Displays and Light Emitting Diode (LED) Display
- 7 Transistors Permit a Wide Range of Applications in Either a Common Emitter (CA3081) or Common Collector (CA3082) Configuration
- High I_C . . . . . 100mA (Max)
- Low V_{CESAT} (at 50mA) . . . . . 0.4V (Typ)

Applications

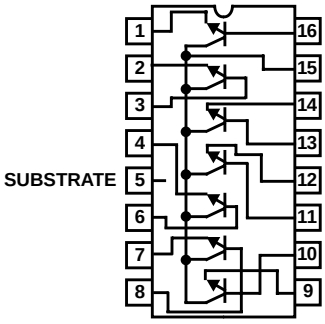
- Drivers for
  - Incandescent Display Devices
  - LED Displays
- Relay Control
- Thyristor Firing

Pinouts

CA3081
COMMON EMITTER CONFIGURATION
(PDIP, CERDIP, SOIC)
TOP VIEW



CA3082
COMMON COLLECTOR CONFIGURATION
(PDIP, SOIC)
TOP VIEW



Absolute Maximum Ratings $T_A = 25^oC$

Collector-to-Emitter Voltage (V_{CEO}) 16V
Collector-to-Base Voltage (V_{CBO}) 20V
Collector-to-Substrate Voltage (V_{CIO}, Note 1) 20V
Emitter-to-Base Voltage (V_{EBO}) 5V
Collector Current (I_C) 100mA
Base Current (I_B) 20mA

Operating Conditions

Temperature Range . . . . . -55^oC to 125^oC

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} ($^oC/W$)	θ_{JC} ($^oC/W$)
CERDIP Package	115	45
PDIP Package	100	N/A
SOIC Package	190	N/A

Maximum Power Dissipation (Any One Transistor) 500mW
Maximum Junction Temperature (Ceramic Package) . . . . . 175^oC
Maximum Junction Temperature (Plastic Package) . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. The collector of each transistor of the CA3081 and CA3082 is isolated from the substrate by an integral diode. The substrate must be connected to a voltage which is more negative than any collector voltage in order to maintain isolation between transistors and provide normal transistor action. To avoid undesired coupling between transistors, the substrate terminal (5) should be maintained at either DC or signal (AC) ground. A suitable bypass capacitor can be used to establish a signal ground.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications For Equipment Design at $T_A = 25^oC$

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C = 500\mu A$, $I_E = 0$	20	60	-	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	$I_C = 500\mu A$, $I_B = 0$	20	60	-	V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	$I_C = 1mA$, $I_B = 0$	16	24	-	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	$I_C = 500\mu A$	5.0	6.9	-	V
DC Forward Current Transfer Ratio	h_{FE}	$V_{CE} = 0.5V$, $I_C = 30mA$	30	68	-	-
		$V_{CE} = 0.8V$, $I_C = 50mA$	40	70	-	-
Base-to-Emitter Saturation Voltage (Figure 4)	V_{BESAT}	$I_C = 30mA$, $I_B = 1mA$	-	0.87	1.2	V
Collector-to-Emitter Saturation Voltage	V_{CESAT}					
CA3081, CA3082		$I_C = 30mA$, $I_B = 1mA$	-	0.27	0.5	V
CA3081 (Figure 5)		$I_C = 50mA$, $I_B = 5mA$	-	0.4	0.7	V
CA3082 (Figure 5)		$I_C = 50mA$, $I_B = 5mA$	-	0.4	0.8	V
Collector Cutoff Current	I_{CEO}	$V_{CE} = 10V$, $I_B = 0$	-	-	10	µA
Collector Cutoff Current	I_{CBO}	$V_{CB} = 10V$, $I_E = 0$	-	-	1.0	µA

Typical Read - Out Driver Applications

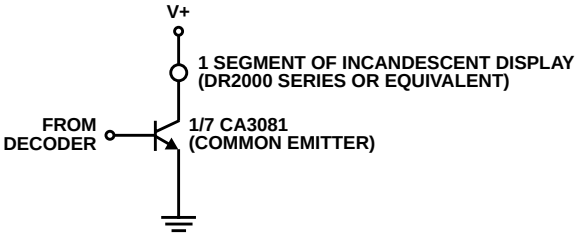
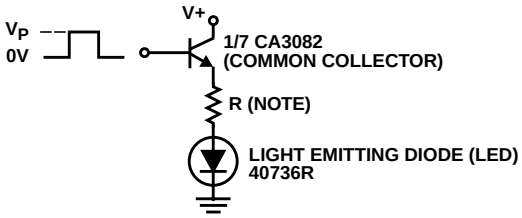


FIGURE 1. SCHEMATIC DIAGRAM SHOWING ONE TRANSISTOR OF THE CA3081 DRIVING ONE SEGMENT OF AN INCANDESCENT DISPLAY



NOTE: The Resistance for R is determined by the relationship:

$$R = \frac{V_P - V_{BE} - V_F(LED)}{I(LED)}$$

$R = 0$ for $V_P = V_{BE} + V_F(LED)$

Where: V_P = Input Pulse Voltage
V_F = Forward Voltage Drop Across the Diode

FIGURE 2. SCHEMATIC DIAGRAM SHOWING ONE TRANSISTOR OF THE CA3082 DRIVING A LIGHT EMITTING DIODE (LED)

Typical Performance Curves

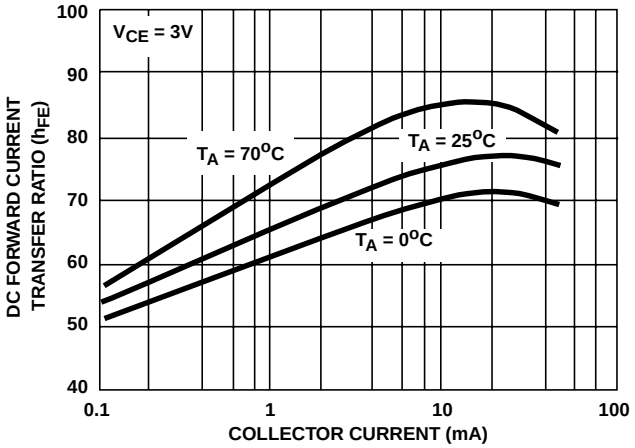


FIGURE 3. DC FORWARD CURRENT TRANSFER RATIO vs COLLECTOR CURRENT

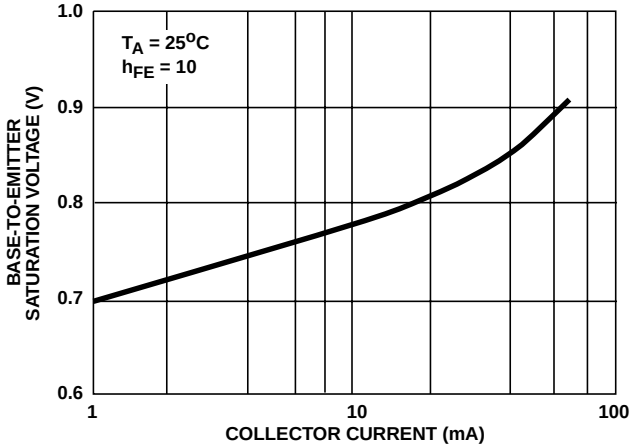


FIGURE 4. BASE-TO-EMITTER SATURATION VOLTAGE vs COLLECTOR CURRENT

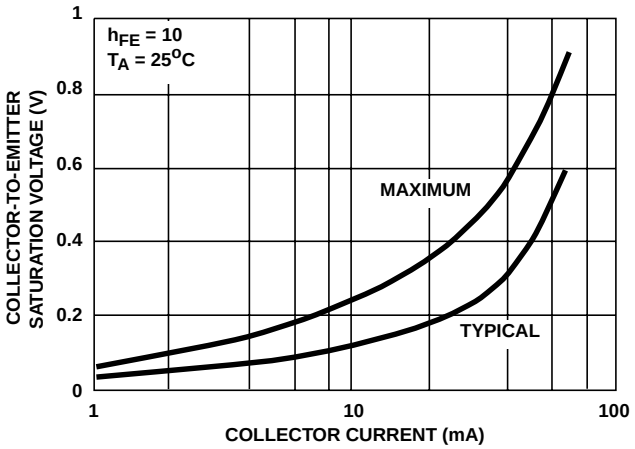


FIGURE 5. COLLECTOR-TO-EMITTER SATURATION VOLTAGE vs COLLECTOR CURRENT

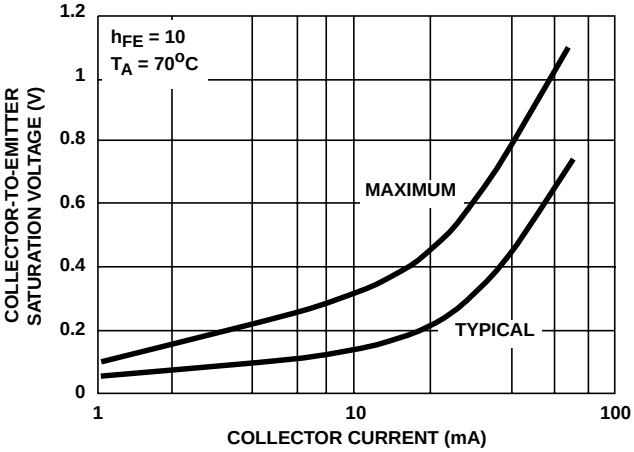
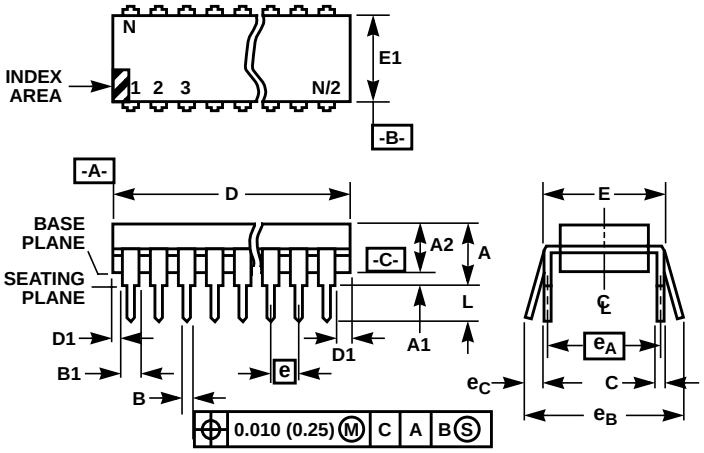


FIGURE 6. COLLECTOR-TO-EMITTER SATURATION VOLTAGE vs COLLECTOR CURRENT

Dual-In-Line Plastic Packages (PDIP)



NOTES:

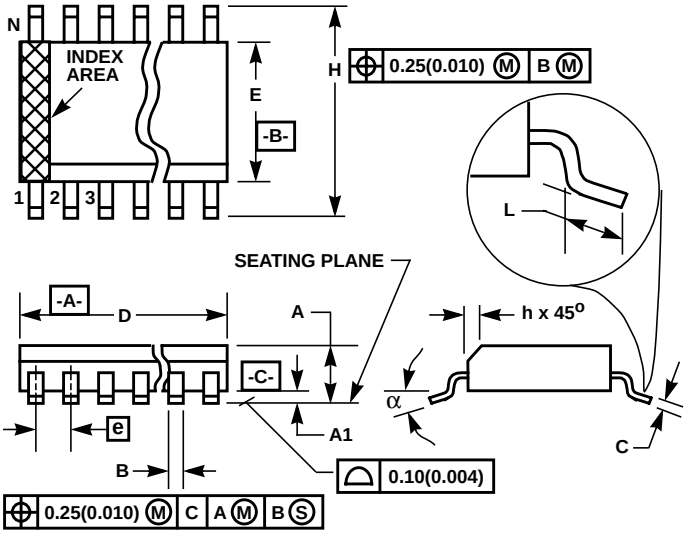
1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E16.3 (JEDEC MS-001-BB ISSUE D)
16 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8, 10
C	0.008	0.014	0.204	0.355	-
D	0.735	0.775	18.66	19.68	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	16		16		9

Rev. 0 12/93

Small Outline Plastic Packages (SOIC)



NOTES:

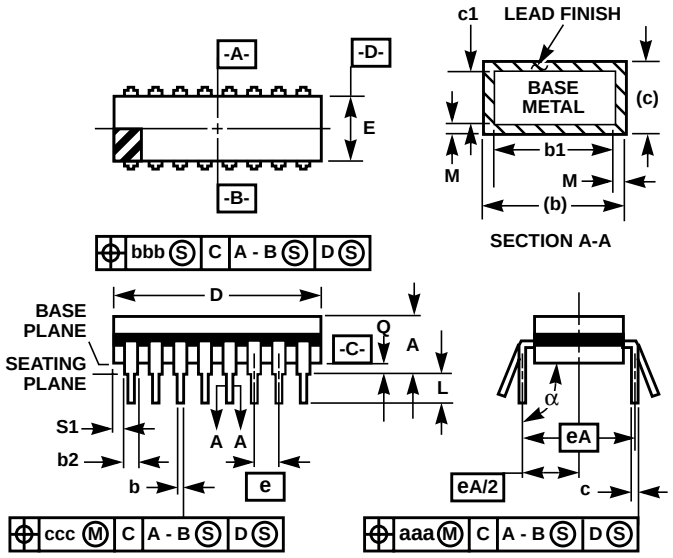
1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M16.15 (JEDEC MS-012-AC ISSUE C)
16 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.3859	0.3937	9.80	10.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	16		16		7
α	0^o	8^o	0^o	8^o	-

Rev. 0 12/93

Ceramic Dual-In-Line Frit Seal Packages (CERDIP)



NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. N is the maximum number of terminal positions.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.

F16.3 MIL-STD-1835 GDIP1-T16 (D-2, CONFIGURATION A)
16 LEAD CERAMIC DUAL-IN-LINE FRIT SEAL PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.840	-	21.34	5
E	0.220	0.310	5.59	7.87	5
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	6
S1	0.005	-	0.13	-	7
α	90^o	105^o	90^o	105^o	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2, 3
N	16		16		8

Rev. 0 4/94

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